

A HIGH-YIELD MONOLITHIC X-BAND FOUR BIT PHASE-SHIFTER

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ABSTRACT

A key element in a GaAs MMIC Transmit/Receive module for active Phased-array application is the phase-shifter needed for the electronic beam steering; because of the circuit complexity and usually large chip size the technological and electrical yield must be maximized. In the present work the design, realisation and performance of an X-band, four-bit phase shifter, using a high-yield technology and a tolerant electric circuit are described.

Keywords: Phase-shifter, Active Phased-array, Electronic Beam Steering, MMIC technology, Switched-line Phase-shifter

1. INTRODUCTION

This work is set in a wide program concerning the realisation of an X-band active phased array S.A.R. antenna for space applications. The central frequency is 9.6 GHz with 100 MHz bandwidth, and the beam steering requires a 4 bit phase-shifter.

Because of the moderate bandwidth and the high operating frequency, the chosen electrical configuration is the switched-line phase-shifter.

2. DESIGN CRITERIA

The electrical design was based on researching and optimizing phase shifter topology not only for RF performance, but also for process insensitivity and high yield. With this purpose we simplified the lay-out minimizing the number of active devices. Furthermore, rather than optimize the single switching element with usual SPDT cells (i.e. with series and shunt FET), and then connect them with the proper electrical length of transmission line, the design method involved the overall optimization of the single bit network.

In particular we chose series switching elements because, when compared with shunt configuration, a chip size minimization and via-holes grounding elimination is obtained. The FET parasitics were tuned in order to meet the operating frequency and bandwidth requirements.

The chosen electrical configuration has the further advantage of being symmetrical, so technological variations have a moderate effect on the electrical yield, i.e. on the differential phase performances.

2.1 I.L. minimization

Fig.1 shows the circuit to be analyzed which consists of a generator connected to a load via two separate paths. Access to these paths is controlled by the impedances Z_H and Z_L , respectively for path 1 and path 2. If Z_L is made small and Z_H is made large, energy propagates from the generator to the load via path 1. Complementary switching of the two impedances causes most of the energy to take the alternate path to the load. If the ratio Z_H/Z_L is very large, at central frequency the difference in path electrical lengths gives a differential phase shift. Such ideal behaviour is not obtained in practice, so the actual value of phase shift and attenuation is affected by the R.F. leakage between the two paths. The total optimization of single bit, comprehensive of active devices (fig. 2), is needed to maximize the quality factor $\Delta\phi/I.L.$ In this work we will show the existence of an I.L. minimum depending on a particular gate width value w_{OPT} . The optimum condition can be found by applying to the circuit the even and odd mode analysis, allowed by the network symmetry about the line shown in fig.1. Fig. 3a and 3b show the application of such analysis to the 180° bit where $\omega_0 = 1/\sqrt{L_1 C_{FET}}$ and $\theta_1 = 0$, $\theta_2 = \pi/2$.

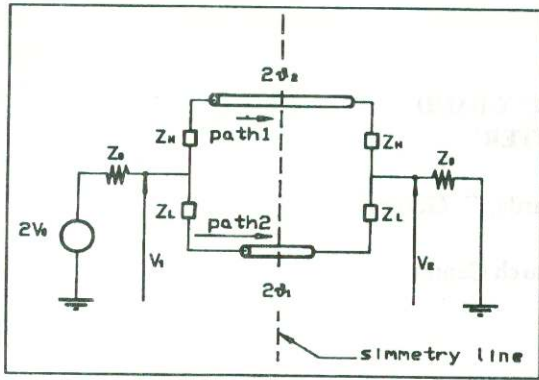


Figure 1: General scheme of Switched Line Phase Shifter

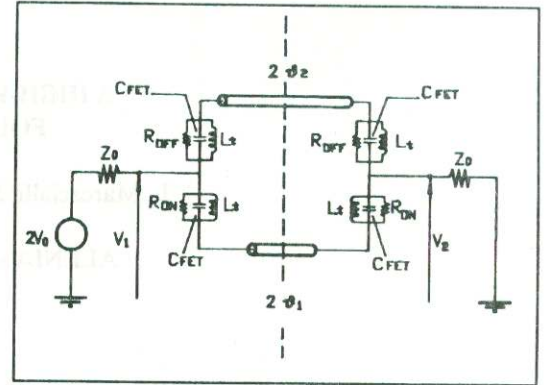


Figure 2: Single bit with active devices equivalent circuit

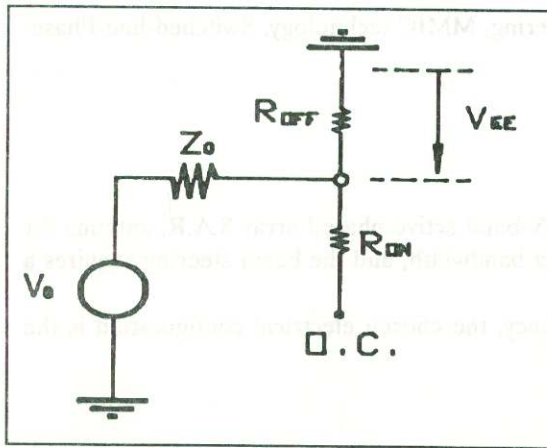


Figure 3a: Even mode for 180° bit at ω_0

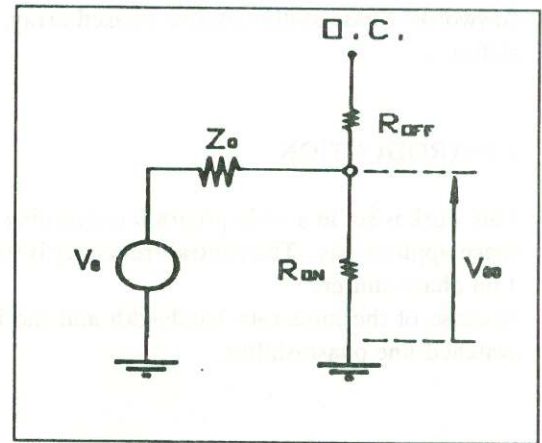


Figure 3b: Odd mode for 180° at ω_0

The voltages V_1 and V_2 in fig.1 are related to the even and odd voltages, V_{EE} and V_{OO} , and in the case of 180° bit we have:

$$V_{EE} = \frac{V_0 R_{OFF}}{Z_0 + R_{OFF}} \quad (1)$$

$$V_{OO} = \frac{V_0 R_{ON}}{Z_0 + R_{ON}} \quad (2)$$

Since

$$V_2 = V_{EE} - V_{OO} \quad (3)$$

and

$$I.L. = 20 \log \frac{V_0}{V_2} \quad (4)$$

for the attenuation we obtain:

$$I.L._{180^\circ} = 20 \log \frac{(Z_0 + R_{OFF})(Z_0 + R_{ON})}{Z_0(R_{OFF} R_{ON})} \quad [dB] \quad (5)$$

If we define:

$$R_{ON} = \frac{r_{ON}}{w} \quad (6)$$

$$R_{OFF} = \frac{r_{OFF}}{w} \quad (7)$$

where w is the gate width and r_{ON} , r_{OFF} are the resistances of $1 \mu m$ gate width in the two possible states, we can introduce a technology dependent ratio

$$k(\omega) = \frac{R_{OFF}(\omega)}{R_{ON}} = \frac{r_{OFF}(\omega)}{r_{ON}} \quad (8)$$

where we assume, in first approximation, that R_{ON} is frequency independent. With these statements at a fixed frequency Eq (5) becomes:

$$I.L._{180^\circ} = 20 \log \frac{(wZ_0 + k r_{ON})(wZ_0 + r_{ON})}{w r_{ON} Z_0 (k-1)} \quad [dB] \quad (9)$$

Applying the minimum condition

$$\frac{d I.L.}{d w} = 0 \quad (10)$$

we obtain the w value for 180° bit:

$$w_{OPT} = \frac{r_{ON} \sqrt{k}}{Z_0} \quad (11)$$

This final result is interesting because the minimum condition for the attenuation depends only on technological parameters, r_{ON} and k . In fig.4 the graph $I.L.$ vs R_{ON} referring to Alenia technology is shown.

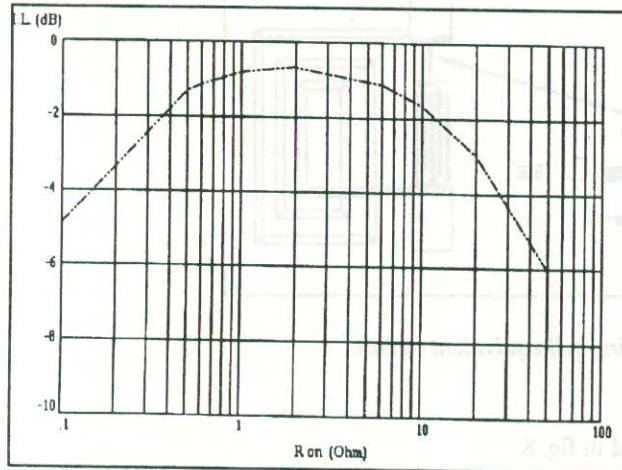


Figure 4: 180° bit $I.L.$ vs R_{on}

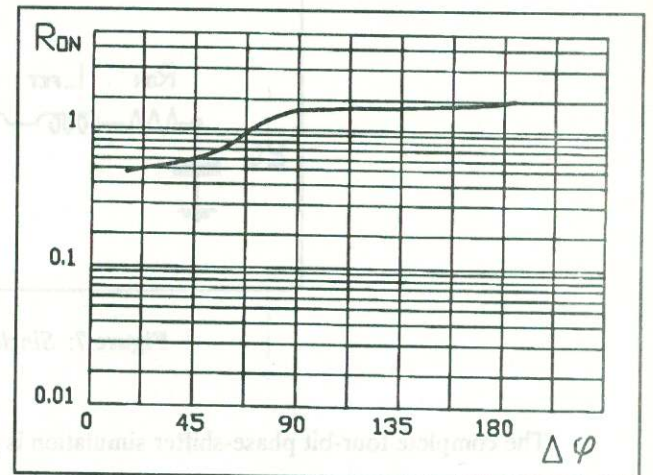


Figure 5: $I.L.$ minima loci for any phase

In the same way, for every phase bit, it is possible to define a function $I.L.(w)$ and to find, with more tedious calculations, the optimum value of gate width which minimizes the attenuation; the I.L. minima loci for any phase are shown in fig 5.

2.2 Layout optimization

The simple FET equivalent circuit shown in fig. 2 is only useful in the I.L. minimum search when the resonance condition has to be imposed, but it does not represent the complete X band behaviour of the tuned FET. In fact, when the design involves the junction layout, a more complex FET equivalent circuit must be used (fig. 6).

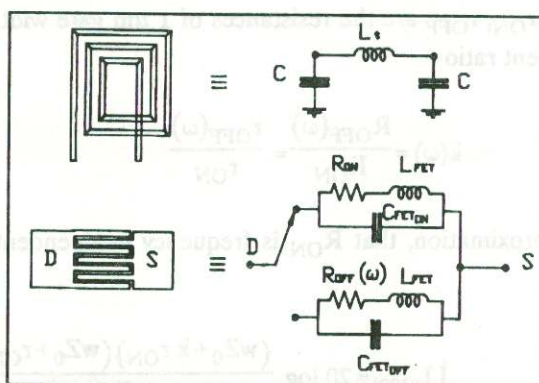


Figure 6: Equivalent circuit of a series FET tuned by a spiral inductor

The FET parasitic reactances L_{FET} and C_{FET} depend on the number of fingers, on their length, on the finger metallization width and on the FET connection with the passive circuit. The tuning inductor parasitic capacitances C , depend on the spiral inductor area and on the ground plane distance.

The layout optimization involved the parasitics effects minimization or absorption in order to obtain a good single bit VSWR to avoid interaction among bits. Several layout solutions have been adopted; among these an inductance L has been added to compensate the effect of tuning inductor parasitic capacitances, making the single switching cell, in the on state, similar to a low-pass network. The inductor has been realized with a short length high impedance transmission line. The equivalent circuit is shown in fig. 7 where the resonant elements are not indicated.

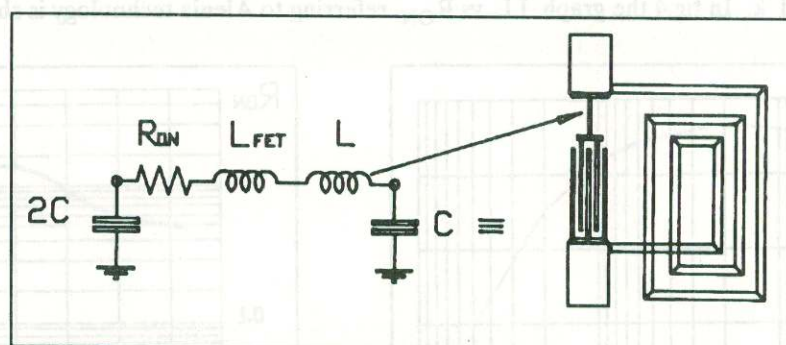


Figure 7: Single switching cell equivalent circuit

The complete four-bit phase-shifter simulation is reported in fig. 8.

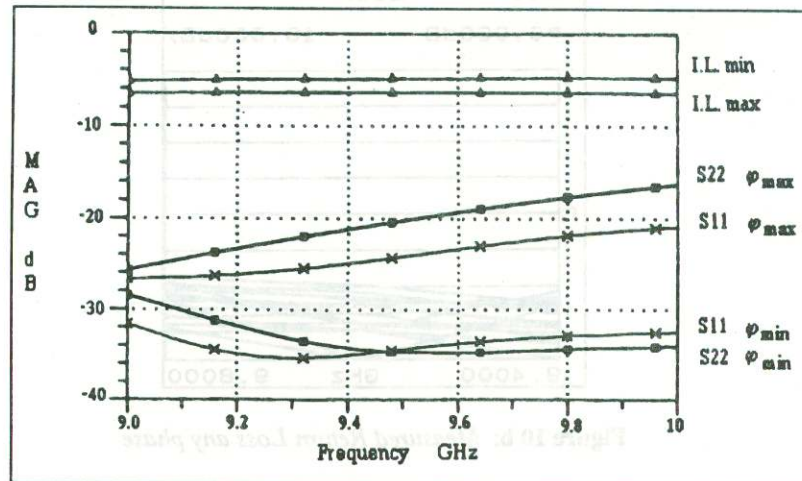


Figure 8: Four bit phase shifter simulation

3. PHASE SHIFTER FABRICATION AND PERFORMANCES

The phase-shifter, utilizing sixteen MESFETs, has been realized on 120 μ m thick GaAs substrate with Alenia standard 0.5 μ m gatelength MMIC technology. We chose a 1200 μ m gate width for each FET as a trade off between minimum I.L. and layout constraints. The photograph of the 5.8 x 3.2 mm chip is shown in fig. 9, whilst the electrical performances are reported in fig.10 a,b and c.

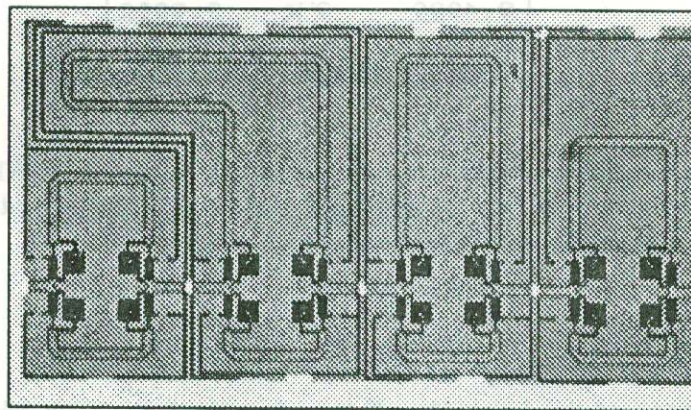


Figure 9: Photograph of Alenia MMIC phase shifter

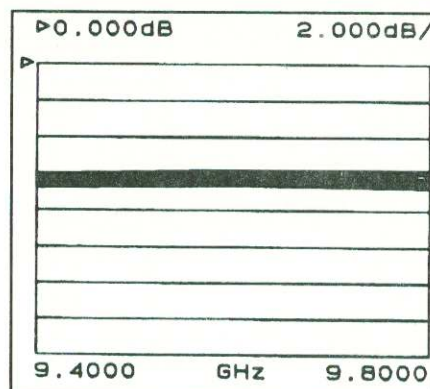


Figure 10 a: Measured I.L. any phase

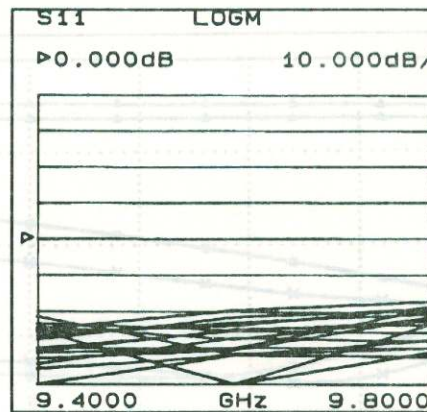


Figure 10 b: Measured Return Loss any phase

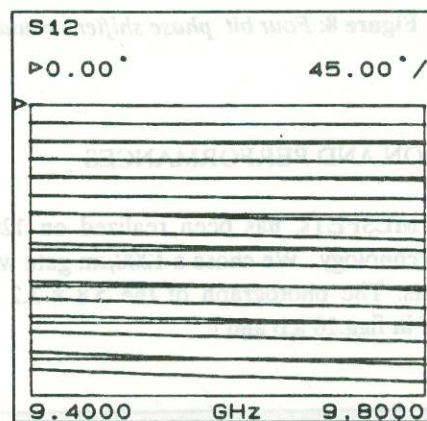


Figure 10 c: Measured Phase Shift

The agreement between simulation and performances, particularly as regards VSWR , shows a good control of junction electrical discontinuities and then the possibility of utilizing in the future the theoretical w_{OPT} value for minimum I.L. without compromising VSWR performances.

4. CONCLUSIONS

In this work we have discussed the design of an X band four-bit phase-shifter, whose simple topology allows, besides high yield, the optimization of the quality factor $\Delta\phi/I.L.$ by means of a theoretical approach. By applying this design method we have fabricated a MMIC phase-shifter with I.L. less than 6.6 dB and VSWR better than 20 dB, any phase.



Figure 10 d: Measured I.L. any phase